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(54) **A surface discharge plasma display panel**

Plasmaanzeigetafel mit Oberflächenentladung

Panneau d'affichage à plasma à décharge de surface

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(73) Proprietor: **FUJITSU LIMITED**
Kawasaki-shi, Kanagawa 211-8588 (JP)

(72) Inventors:
- **Nanto, Toshiyuki**
  Nakahara-ku, Kawasaki-shi, Kanagawa, 211 (JP)
- **Nakahara, Hiroyuki**
  Nakahara-ku, Kawasaki-shi, Kanagawa, 211 (JP)
- **Awaji, Noryuki**
  Nakahara-ku, Kawasaki-shi, Kanagawa, 211 (JP)
- **Wakitani, Masayuki**
  Nakahara-ku, Kawasaki-shi, Kanagawa, 211 (JP)
- **Shinoda, Tsutae**
  Nakahara-ku, Kawasaki-shi, Kanagawa, 211 (JP)
- **Konno, Keiichiro**
  Nakahara-ku, Kawasaki-shi, Kanagawa, 211 (JP)
- **Yanagibashi, Yasuo**
  Nakahara-ku, Kawasaki-shi, Kanagawa, 211 (JP)
- **Sakamoto, Naohito**
  Nakahara-ku, Kawasaki-shi, Kanagawa, 211 (JP)

(74) Representative: **Billington, Lawrence Emlyn et al**
Haseltine Lake & Co.
Imperial House
15-19 Kingsway
London WC2B 6UD (GB)

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Description

[0001] The present invention relates to a surface discharge plasma display panel (hereinafter referred to as a surface discharge PDP) having a matrix display form.

[0002] The surface discharge PDPs are PDPs wherein paired display electrodes defining a primary discharge cell are located adjacent to each other on a single substrate. Since such PDPs can serve adequately as color displays by using phosphors, they are widely used as thin picture display devices for television. And since, in addition, PDPs are the displays that are the most likely to be used as large screen display devices for high-vision pictures, there is, under these circumstances, a demand for PDPs for which the quality of their displays has been improved by increasing resolution and screen size, and by enhancing contrast.

[0003] Fig. 14 is a cross sectional view of the internal structure of a conventional PDP 90. A PDP 90 is a surface discharge PDP having a three-electrode structure and a matrix display form, and is categorized as a reflection PDP according to the form of its phosphors arrangements.

[0004] On the front of a PDP 90, on an internal surface of a glass substrate 11, paired display electrodes X and Y are positioned parallel to each other and arranged for each line of a matrix display so that they cause a surface discharge along the surface of the glass substrate 11. A dielectric layer 17, for AC driving, is formed to cover the paired display electrodes X and Y and separate them from a discharge space 30. A protective film 18 is formed on the surface of the dielectric layer 17 by evaporation. The dielectric layer 17 and the protective flm 18 are transparent.

[0005] Each of the display electrodes X and Y comprises a wide, linear transparent electrode 41, formed of an ITO thin film, and a narrow, linear bus electrode 42, formed of a thin metal film (Cr/Cu/Cr). The bus electrode 42 is an auxiliary electrode used to acquire an appropriate conductivity, and is located at the edge of the transparent electrode 41, away from the plane discharge gap. With such an electrode structure, the blocking of display light can be reduced to the minimum, while the surface discharge area can be expanded to increase the light emission efficiency.

[0006] At the rear, an address electrode A is provided on the internal surface of a glass substrate 21 so that it intersects at a right angle the paired display electrodes X and Y. A phosphors layer 28 is formed on and covers the glass substrate 21, including the upper portion of the address electrode A. A counter discharge between the address electrode A and the display electrode Y controls a condition wherein wall charges are accumulated in the dielectric layer 17. When the phosphors layer 28 is partially excited by an ultraviolet ray UV that occurs as a result of a surface discharge, it produces visible light emissions having predetermined colors. The visible light emissions that are transmitted through the glass substrate 11 constitute the display light.

[0007] A gap S1 between paired display electrodes X and Y arranged in a line is called a "discharge slit," and the width w1 of the discharge slit S1 (the width in the direction in which the paired display electrodes X and Y are arranged opposite each other) is so selected that a surface discharge occurs with a drive voltage of 100 to 200 v applied to the display electrodes. A gap S2 between a line of paired electrodes X and Y and an adjacent line is called a "reverse slit," and has a width w2 greater than the width w1 of the discharge slit S1, that is sufficient to prevent a discharge between the display electrodes X and Y that are arranged on opposite sides of the reverse slit S2. Since paired display electrodes X and Y are arranged in a line with a discharge slit S1 between them, and a line is separated from another line by reverse slits S2, each of the lines can be rendered luminous selectively. Therefore, portions of the display screen that correspond to the reverse slite S2 are non-luminous areas or non-display areas, and the portions that correspond to the display slits S1 are luminous areas or display areas.

[0008] From the front of a conventional panel structure, a phosphors layer 28 in the non-luminescent state is visible through the reverse slits S2. And the phosphors layer 28 in the non-luminescent state has a white or light gray color. Therefore, when a conventional display panel is used in an especially bright place, external light is scattered at the phosphors layer 28 and the non-luminescent areas between lines has a whitish color, which results in the deterioration of the contrast of the display.

[0009] As a method for increasing the contrast for a color display PDP, proposed are a method for providing a color filter by coating the outer surface of the substrate 11 on the front with a translucent paint that corresponds to the luminous color of a phosphors; a method for arranging on the front face of a PDP a filter that is fabricated separately; and a method for coloring a dielectric layer 17 with colors R, G and B.

[0010] It is, however, very difficult to apply coats of individually colored paints at locations corresponding to minute pixels. In case of the separate filter on the front, a gap between the PDP and the filter causes distortion in display images. And in case of the coloring of the dielectric layer 17, since the tints of coloring agents (pigments) differ, uniformity of permitivity is deteriorated by coloring, and a discharge characteristic is rendered unstable. In addition, positioning is also difficult when coloring a dielectric layer, just as the coating of colored paints.

[0011] JP 04 298936 A discloses a surface discharge plasma display panel as set out in the precharacterising part of attached claim 1, wherein light shielding means are provided in the form of eaves on the front surface of a front substrate, to shield phosphors provided on the rear surface of the front substrate.

[0012] JP 04 067534 A discloses circular metal light

shielding layers shielding spacers in the discharge gap of a plasma display panel which is not of the surface discharge type, whilst another such non-surface discharge panel according to JP 60 009029 A comprises shielding masks 10 to shield against light reflected from the side surfaces of spacers between front and rear substrates.

[0013] JP 55 150526 A discloses a gas discharge display device wherein blackened films are provided to suppress the leakage of light emission from pilot discharges in the device.

[0014] None of the above-mentioned documents provides a solution for shielding the reverse slits between pairs of display electrodes on a single substrate of a surface discharge plasma display panel.

[0015] Embodiments of the present invention are intended to increase display contrast while rendering unnoticeable non-luminous areas between lines.

[0016] Embodiments may further provide an optimal structure for forming a light shielding film including black pigment in non-luminous areas between display lines.

[0017] According to the present invention there is provided a surface discharge plasma display panel, having a front substrate and a rear substrate with a discharge space therebetween, and a plurality of pairs of display electrodes extending along respective display lines, wherein a reverse slit where no surface discharge occurs is defined between each adjacent pair of display electrodes and a discharge slit for surface discharge is defined between display electrodes of each single pair thereof, and further wherein a plurality of phosphors extending in bands are provided, and a plurality of address electrodes are provided on the rear substrate, with the phosphors and address electrodes extending along directions crossing the direction of extent of the plurality of pairs of display electrodes, the surface discharge plasma display panel further comprising light shielding means for shielding light hitting the front substrate, characterised in that the display electrodes are formed on the front substrate, the phosphors are provided on the rear substrate, and the light shielding means is a light shielding film positioned between the front substrate and the phosphors, the light shielding film extending in bands which have the same direction of extent as the display electrodes and which are arranged at the reverse slits for shielding light penetration between the front substrate and the rear substrate.

[0018] The area corresponding to a gap (hereinafter referred to as a "reverse slit") between the display electrodes in adjacent lines on a display screen is a non-luminous area. The light shielding film is arranged to correspond with each non-luminous area. Since the plane pattern of the individual shielding films is formed in a belt shape, a striped shielding pattern is formed for the entire display screen. The shielding film blocks visible lights that may be transmitted through the reverse slits. Therefore, the occurrence of a phenomenon where non-luminous areas appear bright due to the external light and a leaking light from display lines may be prevented so that the display contrast is increased.

[0019] According to one embodiment of the present invention, there is provided a surface discharge plasma display panel, wherein paired display electrodes are formed for each display line on an internal surface of a front substrate extending along the display lines, and phosphor is deposited on the internal surface of a rear substrate, and wherein a light-shielding film having a darker color than the phosphors with non-luminous condition and having a belt shape extending in the display line direction is formed on the internal surface of the front substrate, so as to overlap each area sandwiched between the adjacent display electrodes.

[0020] When viewing the display screen from the front, the phosphors layer is hidden by the shielding film in the non-luminous areas that correspond to the reverse slits.

[0021] According to a second embodiment of the present inwntion, there is provided a plasma display panel wherein display electrodes are covered and separated from a discharge space by a dielectric layer, and a light shielding film is located between the front substrate and the dielectric layer.

[0022] According to a third embodiment of the present invention there is provided a plasma display panel wherein each display electrode comprises a transparent electrode and a metal electrode, which is narrower than the transparent electrode and which overlaps the edge of the transparent electrode at a location close to the non-luminous area, and wherein a light shielding film is located at the front of the display electrode in the substrate facing direction so as to overlap the metal electrodes on both sides of the non-luminous area.

[0023] Since the shielding film is also provided on the front of the metal electrode, the deterioration of display quality due to the reflection of external light from the surfaces of metal electrodes can be reduced, perhaps significantly.

[0024] An embodiment of the present invention may be made by a method of manufacturing a plasma display panel wherein the display electrodes and the light shielding film are formed on the front substrate, a coating of dielectric material is applied to form the dielectric layer, and the resultant structure is annealed. This coating and annealing process is performed twice. The thickness of the first coating is selected to be smaller than the second coating.

[0025] Since the thickness of the first dielectric coating subject to the first annealing is thin, a floating and moving of the shielding film through the softening of the dielectric material during the first annealing can be minimized so that an unnecessary extending of the shielding film toward the display electrodes to cover them can be avoided.

[0026] An embodiment of the invention may also be made by a method of manufacturing a plasma display panel wherein the display electrodes and the light

shielding film are formed on the front substrate, a coating of dielectric material is applied to form the dielectric layer, and the resuultant structure is annealed. This coating and annealing process is performed twice. The first annealing temperature is set so that it is lower than the temperature at which the dielectric material is softened.

[0027] By setting the annealing temperature lower than the softening temperature, the unwanted expansion of the shielding film to cover the display electrodes can be prevented.

[0028] Further, the above method for manufacturing a plasma display panel may comprise the steps of:

depositing a light shielding material on a front substrate and performing patterning to form a light shielding film;
forming a transparent conductive film on the front substrate on which the light shielding film is formed, and performing patterning to provide a transparent electrode that partially overlaps the light shielding film;
painting a photosensitive material, which is insolubilized by exposure to light, to cover the light shielding film and the transparent electrode, exposing the photosensitive material as a whole from the reverse face of the front substrate and developing the photosensitive material to form a resist layer between the light shielding films; and
selectively forming a metal electrode on the exposed portion of the transparent electrode by plating it with a metal film. By using this method, self-alignment of the light shielding film and the metal electrode is performed.

[0029] An embodiment of the inventive plasma display panel may have a pair of substrates facing each other with a discharge space therebetween, wherein paired display electrodes, extending along display lines are formed for each display line on an internal surface of one of the pair substrates so that a discharge is performed between the paired display electrodes; and wherein a light shielding film having a stripe shape and extending along display lines is formed in an area between the display lines and sandwiched between the pair diplay electrodes on the internal surface of one of the substrates, so that the light shielding film is separated from the display electrodes.

[0030] The light shielding film may be formed so as to partially overlap over the display electrodes.

[0031] With an arrangement wherein the display electrodes are formed first and thereafter the light shielding film is formed, the manufacture of display electrodes using a high vacuum process, such as sputtering, is more easily performed.

[0032] Another method for manufacturing a plasma display panel having a pair of substrates facing each other with a discharge space therebetween, may comprise the steps of:

forming a plurality of pair display electrodes on one of the pair substrates to form display lines therebetween;
forming a film containing a dark pigment on the display electrodes on the substrate, and performing patterning of the film so that a stripe shaped light shielding film, extending along the display lines, is provided in an area between the display lines and sandwiched between the pair display electrodes; and
forming a dielectric paste film on the display electrodes and the light shielding film, and annealing the resultant structure at a predetermined temperature.

[0033] In all cases the contrast of the display under bright external conditions is increased by having a light shielding film extending in bands in betwen the display lines within the structure of the plasma display genel.

[0034] For a better understanding of the invention and to show how it may be put into effect reference will now be made, by way of example, to the accompanying drawings in which:

Fig. 1 is a perspective view illustrating the basic structure of a PDP relating to the present invention;
Fig. 2 is a cross sectional view of the essential portion of the PDP according to a first embodiment;
Fig. 3 is a plan view of a light shielding film;
Figs. 4A through 4F are diagrams illustrating a method for fabricating the front portion of the PDP;
Fig. 5 is a cross sectional view of the essential portion of a PDP according to a second embodiment of the present invention;
Fig. 6 is a cross sectional view of the essential portion of a PDP according to a third embodiment of the present invention;
Fig. 7 is a cross sectional view of the essential portion of a PDP according to a fourth embodiment of the present invention;
Fig. 8 is a cross sectional view of the essential portion of a PDP according to a fifth embodiment of the present invention;
Figs. 9A through 9E are cross sectional views for explaining a method for manufacturing the PDPs of the second, the fourth and the fifth embodiments of the present invention;
Figs. 10A through 10C are cross sectional views for explaining a method for manufacturing the PDPs of the second, the fourth and the fifth embodiments of the present invention;
Fig. 11 is a plan view of a PDP wherein a light shielding film is also formed in a periphery of a display area of the panel;
Fig. 12 is a cross sectional view of a portion taken along the line XX-YY in Fig. 11;
Fig. 13 is a cross sectional view of a modification of

the PDP; and

Fig. 14 is a cross sectional view of the essential portion of the internal structure of a conventional PDP.

[0035] Fig. 1 is a perspective view illustrating the basic structure of a PDP 1 according to the present invention. The same reference numerals as used in Fig. 14 are also used in Fig. 1 to denote corresponding or identical components, regardless of differences in shapes and materials. The same can be applied for the following drawings.

[0036] The PDP 1, as well as the conventional PDP 90, is a surface discharge PDP having a three-electrode structure with a matrix display form, that is called a reflection type. The external appearance is derived from paired glass substrates 11 and 21, which face each other with an intervening discharge space 30 therebetween. The glass substrates 11 and 21 are bonded by a seal frame layer (not shown) of a glass having a low-melting point that is formed along the edges of the facing substrate.

[0037] A pair of linear display electrodes X and Y in parallel are arranged for each line L of a matrix display on the internal surface of the front glass substrate 11, for the generation of a surface discharge along the substrate surface. The line pitch is, for example, 660 μm.

[0038] Each of the display electrodes X and Y comprises a wide, linear transparent electrode 41 formed of ITO thin film and a narrow, linear bus electrode 42 formed of metal thin film having a multi-layer structure. As specific example sizes, the transparent electrode 41 is 0.1 μm thick and 180 μm wide, while the bus electrode 42 is 1 μm thick and 60 μm wide.

[0039] The bus electrode 42 is an auxiliary electrode for acquiring appropriate conductivity, and is located at the edge of the transparent electrode 41 away from a surface discharge gap.

[0040] For the PDP 1, a dielectric layer for (example PbO low-melting-point glass layer) 17 for AC driving is formed to cover the display electrodes X and Y and separate them from the discharge space 30. A protective film 18 made of MgO (magnesium oxide) for example is deposited on the surface of the dielectric layer 17 by evaporation. The thickness of the dielectric layer 17 is about 30 μm and the thickness of the protective film 18 is approximately 5000 Å for example.

[0041] The internal surface of the rear glass substrate 21 is coated with an underlayer 22 of approximately 10 μm, which is ZnO low-melting-point glass for example. Address electrodes A are arranged on the underlayer 22 at constant pitches (for example 220 μm), so that they intersect the paired display electrodes X and Y at a right angle. The address electrode A is produced by annealing silver paste for example, and its thickness is about 10 μm. The underlayer 22 prevents electromigration of the address electrodes A.

[0042] The condition of wall electric charge accumulation on the dielectric layer 17 is controlled by a discharge between the address electrodes A and the display electrodes Y. The address electrodes are also covered with a dielectric layer 24 that is formed of low-melting-point glass with the same composition for example as that of the underlayer 22. The dielectric layer 24 at the upper portions of the address electrodes A is about 10 μm thick for example.

[0043] On the dielectric layer 24, a plurality of barrier ribs 29, which are about 150 μm high and linear in a plan view, are individually arranged between the address electrodes A.

[0044] Then, phosphors layers 28R, 28B and 28C (hereinafter referred to as the "phosphors layers 28," when distinguishing between colors is not especially required), for the three primary colors R (red), G (green) and B (blue) of a full-color display, are formed so as to cover the surface of the dielectric layer 24, including the upper portions of the address electrodes A, and the sides of the barrier ribs 29. These phosphors layers 28 emit light when they are excited by the ultraviolet rays produced by the surface discharge.

[0045] The discharge space 30 is defined by the barrier ribs 29 for the units of light emitting areas along the lines (along the arrangement of pixels running parallel with the display electrodes X and Y), and the size of a gap between the discharge space 30 is also defined. In the PDP 1, there are no barrier ribs for defining the discharge space 30 along the columns for a matrix display (along the arrangement direction of the paired display electrodes X and Y or the address lines direction). However, since the size of a gap (the width of a reverse slit) for display lines L, along which the paired display electrodes X and Y are arranged, is set to from 100 to 400 μm, sufficiently large compared with the size of a surface discharge gap (the width of a discharge slit) of 50 μm for each display line L, the interference of a discharge does not occur between the lines L.

[0046] A display pixel of the PDP 1 comprises three unit light emitting areas (sub-pixels) adjacent each other in each line L. The luminous colors for all the lines L in the same column are the same, and the phosphors layers 28R, 28B and 28C are so provided by screen printing that they are continuously arranged in each column along the address electrode. For this, screen printing provides excellent productivity. Compared with an arrangement wherein the phosphors is divided for each line L, the arrangement of the continuous phosphors layers 28 along a column can easily provide the uniform thickness of the phosphors layers 28 for the sub-pixels.

[0047] Fig. 2 is a cross sectional view of the essential portion of the PDP 1, and Fig. 3 is a plan view of a light shielding film 45. As is shown in Fig. 2, a light shielding film 45 for blocking (shielding) a visible light is formed for each reverse slit S2, so that the film 45 directly contacts the internal surface of the glass substrate 11. As is shown in Fig. 3, the shielding films 45 are formed in patterns of belts or strips that extend along the display lines, and are located to overlap the areas sandwiched

between the display electrodes X and Y of the adjacent lines L. The light shielding films 45 separated from each other constitute a striped shielding pattern for an entire display screen, so that the phosphors layers 28 are hidden between the display lines L and the contrast for a display is increased. Since the striped pattern along the display line L does not shift along the display lines L , unlike a matrix pattern surrounding the sub-pixels or pixels, it is easy to align and position the glass substrates 11 and 21 during the manufacturing of the PDP 1.

[0048] It is preferable that the top portions of the barrier ribs 29 have the same dark color as that of the light shielding films. A dark lattice pattern is formed by intersecting the barrier ribs and the light shielding films, and the outline of each sub-pixel becomes clear. More specifically, a black color agent, such as chromium (Cr), is mixed with the material for the barrier ribs to provide uniformly dark barrier ribs.

[0049] Figs. 4A through 4F are diagrams illustrating a method for manufacturing the front side portion of the PDP 1. The PDP 1 is produced by providing predetermined components independently for the glass substrate 11 and the glass substrate 21, and by thereafter bonding together the glass substrates 11 and 21 around their circumferences while they are positioned facing each other.

[0050] For fabrication of the front portion, first, a dark colored insulating material is deposited on the surface of the glass substrate 11 by sputtering to form an insulation film (not shown) having a surface reflectivity lower than that of the metal electrode 42. Chromium oxide (CrO) or silicon oxide can be used as the insulation material. It is desirable that the thickness of the insulation film be 1 μm or less in order to reduce the step difference to the transparent electrodes 41. Then, patterning is performed to the insulation film by photolithography using a first light exposing mask, and a plurality of the light shielding film stripes 45 described above are produced at one time (Fig. 4A).

[0051] Sequentially, an ITO film is deposited on the glass substrate 11, whereon the light shielding films 45 are formed, and patterning of the ITO film is performed by photolithography using a second light exposing mask. Transparent electrodes 41 are thus formed so that they partially overlap the light shielding films 45 (Fig. 4B).

[0052] A negative photosensitive material 61, which is irreversibly solidified by exposure to ultraviolet rays, is coated on the resultant structure so that it covers the light shielding films 45 and the transparent electrodes 41. The photosensitive material is fully exposed to the light from the reverse side of the glass substrate 11 (Fig. 4C). Then, the photosensitive material 61 is developed and forms a resist layer 62 which covers only an area between the light shielding films 45 (Fig. 4D).

[0053] Following this, the metal electrodes 42, having a multiple layer structure of, for example, nick-el/copper/nickel, are formed on the exposed portions of the transparent electrodes 41 by selective plating (Fig. 4E).

[0054] The resist layer 62 is removed, and the dielectric layer 17 and the protective film 18 are deposited in order. The front portion of the PDP 1 is thus produced (Fig. 4F).

[0055] In the above described process, the number of required light exposing masks is two (Figs. 4A and 4B), the same as is required by the fabrication process for the conventional PDP 90, and the number of alignment procedures for the exposing masks is one, also the same as in the conventional process. In other words, according to the fabrication method in Fig. 4, the light shielding films 45 can be formed without deterioration of a yield due to a shift in alignment.

[0056] Fig. 5 is a cross sectional view of the essential portion of a PDP 2 according to a second embodiment of the present invention, i.e., showing the front portion of a discharge space. In the PDP 2, light shielding films 46 having the same width as the reverse slit S2 are provided on the internal surface of a front glass substrate 11. As well as the light shielding films 45 in Fig. 3, the light shielding films 46 are extended in a belt shape along the display line in a plan view, and constitute a striped light shielding pattern.

[0057] For fabrication of the PDP 2, paired display electrodes X and Y are formed on the glass substrate 11. And a black pigment, such as iron oxide or cobalt oxide, that has a heat resistance of 600°C or higher is printed on the reverse slit area S2 to form the light shielding films 46. Low-melting-point glass is coated and annealed at 500 to 600°C to produce the dielectric layer 17.

[0058] It is preferable that the thickness of the light shielding films 46 be less than the thickness of the individual display electrodes so as to acquire the flat surface of the dielectric layer 17. Further, it is desirable that the dielectric layer 17 be formed in two layers, and that annealing be performed for each layer. More specifically, a comparatively thin coat of low-melting-point glass paste is applied to the substrate and the glass paste is annealed to form a lower dielectric layer 17a. Then, another coat of the low-melting-point glass paste is applied to acquire a dielectric layer 17 having the required thickness, and the glass paste is annealed to produce an upper dielectric layer 17b. Since the lower dielectric layer 17a, which contacts the light shielding layers 46, is formed thin, the migration of a black pigment caused through the softening of the low-melting-point glass during the annealing, can be reduced, and the reduction in luminance due to the unwanted expansion of the light shielding films 46 can be prevented. When the thickness of the lower dielectric layer 17a is so set that it is one tenth of or less than the width of the light shielding films 46, the migration of the pigment does not substantially appear.

[0059] It should be noted that the unwanted expansion of the light shielding films 46 can also be prevented by setting the temperature for annealing the lower die-

lectric layer 17a to a temperature that is lower than that for softening the low-melting-point glass. In this case, the lower dielectric layer 17a and the upper dielectric layer 17b can be formed with the same thickness, or the upper dielectric layer 17b can be formed thinner than the lower dielectric layer 17a.

[0060] Fig. 6 is a cross sectional view of the essential portion of a PDP 3 according to a third embodiment of the present invention, and shows the structure of the front side portion of the discharge space. In the PDP 3, a light shielding film 47 is provided for each reverse slit S2 in an intermediate portion in the direction of the thickness of a dielectric layer 17. The light shielding film 47, as well as the light shielding films 45 in Fig. 3, are extended in a belt shape along the display line in a plan view, and constitute a striped light shielding pattern.

[0061] A width w47 of the light shielding film 47 is greater than a width w2 of the reverse slit S2, and is smaller than the interval w22 between the edges, which are closer to the discharge slit S1, of the metal electrodes 42 sandwiching the reverse slit S2. In other words, the plane size of the light shield film 47 is so selected that it partially overlaps the metal electrodes 42. With this structure, the light shielding film 47 can be easily positioned so that it fully overlaps the reverse slit S2 and does not overlap the light transmitting portion 41 in the display line. It is also important that the light shielding film 47 is apart from the electrodes 41,42.

[0062] Fig. 7 is a cross sectional view of the essential portions of a PDP 4 according to a fourth embodiment of the present invention. The light shielding films 45 shown in Fig. 2 are formed between the X and Y electrodes 41 and 42 and the front glass substrate 10. In the PDP 4 shown in Fig. 7, light shielding films 49 are formed inside the reverse slit S2 areas between the X and Y electrodes 41 and 42 so that they partially overlap the X and Y electrodes 41 and 42. This structure is similar to that in Fig. 2 because the light shielding films 49 are so formed that they completely hide the reverse slit S2 areas between the display lines L. However, the manufacturing process for this structure differs from that in Fig. 2 in that the light shielding films 49 containing a black pigment are formed after the X and Y electrodes 41 and 42 are provided. This manufacturing process will be described later in detail.

[0063] In the structure of the PDP 4 shown in Fig. 7, it is important for the light shielding films 49 to overlap the electrodes X and Y up to around the middle portions of the bus electrodes 42, which constitute a three-layer structure of Cr/Cu/Cr. In other words, while the bus electrodes 42 provide a higher conductivity for a highly resistant material for the transparent electrodes 41, the electrodes 42 themselves possess light shielding property. When the light shielding films 49 are so formed that they overlap the bus electrodes 42, the portions, except for the display line areas L, are completely shielded.

[0064] Fig. 8 is a cross sectional view of the essential portion of a PDP 5 according to a fifth embodiment of the present invention. In the PDP 5, light shielding films 48 are formed between X and Y electrodes 41 and 42 at a certain interval and without making contact with them. When the distance of the non-display areas between the X and Y electrodes 41 and 42 is 500 μm (using as an example a 42-inch PDP), the light shielding film 48 is formed at an interval of about 20 μm from the electrodes 41 and 42. This structure is preferable from the view of the manufacturing process for it, even though the gap between the display line areas L is not completely closed. More specifically, as well as with the PDP 4 in Fig. 7, the light shielding films 48 can be formed after the X and Y electrodes 41 and 42 are provided. Moreover, the annealing of the light shielding films 48 can be performed in conjunction with the annealing process for the dielectric layer 17, made of a low-melting-point glass, that is formed on them. Since the light shielding films 48 do not contact the electrodes 41 and 42 in the annealing process at a high temperature, a stable process can be accomplished. This will be described later in detail.

[0065] In the structure of the PDP 5 in Fig. 8, since the width of the light shielding films 48 is considerably smaller than the non-display area W22, there is sufficient space so that when the alignment (positioning) of the light shielding films 48 is performed, the films 48 can be easily formed not to overlap the display line areas L.

[0066] Figs. 9A through 9E and 10A through 10C are cross sectional views for explaining a method for respectively fabricating the PDPs of the second, fourth, and fifth embodiments, shown in Figs. 5, 7 and 8.

[0067] As is shown in Fig. 9A, after a silicon oxide film (not shown), for example, is formed as a passivation film on a glass substrate 11, a transparent electrode layer 41 is formed across the entire surface by sputtering. The transparent electrode layer 41 is formed with a thickness of approximately 0.1 μm by using ITO. Then, in the common lithography procedure, the transparent electrode layer 41 is formed in a striped pattern to provide X and Y electrodes 41 having a width of about 180 μm.

[0068] Sequentially, as is shown in Fig. 9B, a metal layer 42 having a three-layer structure of Cr/Cu/Cr is formed as a bus electrode layer of about 1 μm on the entire surface by sputtering. The common lithography procedure is performed to pattern the metal layer 42 to approximately 60 μm. As is previously described, the bus electrode 42 is so formed that it is positioned at the end of the side opposite to the side of the electrode 41 faces each other closely.

[0069] For the formation of the X and Y electrodes 41 and 42, sputtering is performed on the glass substrate 11 after it is placed in a high vacuum chamber. Since a light shielding film containing a black pigment, etc., is not formed on the glass substrate 11, the sputtering under a high vacuum can be stably performed.

[0070] Then, as is shown in Fig. 9C, a photoresist layer 71 containing a black pigment is formed by screen printing. The black pigment is oxide of manganese (Mn),

iron (Fe), or Copper (Cu), for example. Such a pigment is mixed in a photoresist including photosensitive material. For example, a pigment dispersion photoresist (product name: CFPR BK) of Tokyo Ohka Kogyo Co., Ltd. is used.

[0071] Following this, as is shown in Fig. 9D, the resultant structure is exposed to light through a predetermined mask pattern, and developed. Then, baking (drying) is performed on the structure for two to five minutes in a dry atmosphere at 120°C to 200°C, for example, to form the light shielding films 49. In the example shown in Fig. 9D, as for the PDP 4 shown in Fig. 7, the light shielding films 49 is patterned to overlap the X and Y electrodes 41 and 42.

[0072] When a different mask pattern is used, the light shielding films 48 can be formed separately from the X and Y electrodes 41 and 42, as is shown in Fig. 9E. This structure corresponds to that of the PDP 5 shown in Fig. 8. Similarly, the light shielding films 46 can be formed as are shown for the structure in Fig. 5.

[0073] As is described above, a photosensitive resist of a polymer organic material is used for the light shielding films 49 and 48. If, prior to the formation of the electrodes 41 the light shielding films are formed and annealed for stability, the contact of the electrodes 41 may be deteriorated due to an uneven surface of the film. From this point of view, the process in Fig. 9 is an effective one.

[0074] Figs. 10A through 10C are cross sectional views of a method for forming a dielectric layer 17 and a MgO protection layer 18 on light shielding films. An explanation will be given for this example by employing the light shielding films 48, shown in Figs. 8 and 9E, that are formed separately from the electrodes 41 and 42.

[0075] In the fabrication process for the dielectric layer 17 shown in Fig. 10, annealing of the light shielding films 48 is also performed together with the procedure for annealing the dielectric layer 17. For the formation of the dielectric layer 17, a low-melting-point glass paste containing lead oxide (PbO) as the main element is printed on the surface of the substrate, and is then annealed. This process involves at least two procedures: the printing and the annealing of the lower dielectric layer 17a and the upper dielectric layer 17b. Specifically, as a material for the lower dielectric layer 17a, a composition is selected for which the viscosity is not decreased in the annealing atmosphere and which does not easily react with the ITO of the transparent electrodes 41 and the copper (Cu) of the bus electrodes 42. Such a composition material is, for example, a glass paste that comprises $PbO/SiO_2/B_2O_3/ZnO$, and that contains a comparatively large amount of SiO_2.

[0076] As a material for the upper dielectric layer 17b, a composition is selected for which the viscosity is adequately decreased in the annealing atmosphere and the surface is flattened. As such a composition material, a glass paste which comprises $PbO/SiO_2/B_2O_3/ZnO$ and contains a comparatively small amount of SiO_2 is selected.

[0077] As is shown in Fig. 10A, the surface of the glass substrate 11 is printed by a glass paste, which comprises $PbO/SiO_2/B_2O_3/ZnO$ and contains a comparatively large amount of SiO_2. The substrate 11 is then annealed for about 60 minutes in a dry atmosphere at 580°C to 590°C. The viscosity of the glass paste is not much decreased at the annealing temperature, and the paste does not easily react with the ITO of the transparent electrodes 41 and the copper (Cu) of the bus electrodes 42. Further, the glass paste is annealed at the same time as the light shielding films 48. Therefore, a savings in the time and labor required for the annealing process can be realized, as compared with the example wherein the light shielding films 48 are formed prior to the electrodes 41 and 42.

[0078] Next, as is shown in Fig. 10B, the upper dielectric layer 17b is formed. In the same manner as for the lower dielectric layer 17a, the substrate is printed by using a glass paste and is annealed for about 60 minutes in a dry atmosphere at 580°C to 590°C. The preferable glass paste is one that comprises $PbO/SiO_2/B_2O_3/ZnO$ and contains a comparatively small amount of SiO_2, as is described above. As a result, the dielectric layer 17 having a flat surface is formed.

[0079] Finally, a thick layer of low-melting-point glass film for sealing is formed around the edges of the glass substrate 11 (not shown), and then, as is shown in Fig. 10C, the MgO film 18 is formed as a protective film by evaporation.

[0080] Although the light shielding films 48 are formed separately from the electrodes 41 and 42 in the process shown in Fig. 10, as previously described, the light shielding films may contact the electrodes 41 as in the PDPs 2 and 4 shown in Figs. 5 and 7. Though the reason is still not well understood, when a substrate on which light shielding films are in contact with electrodes 41 and 42 is placed in an annealing atmosphere at a temperature close to 600°C, the light shielding films may be turned brown, and to prevent this, it may be effective for the light shielding films to be separated from the electrodes 41 and 42 in the same manner as for the light shielding films 48. The separation interval in this case is called a color change prevention gap for convenience sake.

[0081] Fig. 11 is a plan view of a PDP wherein light shielding films 48 are formed in the periphery outside a display area of the panel. Fig. 12 is a cross sectional view of the portion taken along the line XX-YY in Fig. 11. As is described above, the contrast of a display is increased by forming light shielding films 48 between the X and Y electrodes in the areas between the display lines L1, L2 and L3. In Fig. 11, the light shielding films 48 are also formed in a peripheral area.

[0082] In the PDP, to prevent an occurrence of accidental discharge, dummy X and Y electrodes DX and DY, are formed at the peripheral portions of paired X and Y electrodes X1, Y1, X2, Y2, X3 and Y3, which com-

monly serve as display electrodes. Wall charges not required for display are prevented from being accumulated by frequently performing discharges between the dummy electrodes DX and DY also. The discharges performed in the peripheral area and the exposure of the phosphors layer cause contrast in a display area to be deteriorated. Therefore, as is shown in Fig. 11, the light shielding films 48 are formed on the dummy electrodes DX and DY (indicated as Dummy in Fig. 11), and on a peripheral area PE where leads 42R of bus electrodes 42 are formed. The EX described by the chain lines is a display screen frame on the surface of the panel, and a sealing member 50 is formed at a position on the frame EX to seal the glass substrates. In the cross sectional view in Fig. 12, the front glass substrate 11 and the sealing member 50 formed on the MgO film 18 are shown, while a rear glass substrate is omitted.

[0083] The leads 42R of the bus electrodes 42 are connected to an external controller via a flexible cable (not shown). Therefore, the two glass substrates are sealed together by the sealing member 50 at the portion of the leads 42R of the bus electrodes 42.

[Material for light shielding film]

[0084] An explanation has been given for the process for forming the dielectric layer 17 on the light shielding films 48 and annealing them at about 600°C, as is shown in Figs. 10A through 10C. If the display electrodes and the light shielding films are in contact with each other, the black color of the light shielding films 48 may be changed. Although the reason is not well understood, it seems that the display electrodes and the light shielding films that are in contact with each other tend to be ionized during the annealing process, and the low-melting-point glass paste absorbs oxygen from the oxides of Mn, Fe and Cu, which are contained in the black pigment, and the oxides are reduced. Thus, an effective means to prevent the color change is for an oxide agent actively discharging oxygen to be mixed in the photosensitive resist 71 containing the black pigment, which is formed into the light shielding films.

[0085] The specific oxide agents that were used in this manner are $NaNO_3$, BaO_2, etc. And as a result, it was confirmed that no color change occurred, even when the annealing process was completed.

[0086] The light shielding films can increase the contrast for a display in the PDP by not leaking light to the exterior from inside the PDP. However, because of the black color, external light is regularly reflected from the phase boundary between the light shielding films 48 and the glass substrate 11, and as a mirror image due to this regular reflection appears, it is sometimes difficult to look at the display screen. Even in the conventional structure in which light shielding films are not formed, the regular reflection between the paired display electrodes occurs on the surface of the address electrodes at the back substrate. To prevent the regular reflection from occurring at the phase boundary between the light shielding films 48 and the glass substrate 11, a low-melting-point glass powder is mixed in the material for the light shielding films.

[0087] The low-melting-point glass powder is the same material as the dielectric layer 17, for example, and is contained about 50% in the organic photosensitive resist 71. The organic photosensitive resist 71, therefore, contains a black pigment and low-melting-point glass powder. Although, as in conventional manner, the regular reflection of external light occurs on the outer surface of the front glass substrate 11, the refractive index of the light shielding film 48 is close to that of the glass substrate 11 at their phase boundary, and accordingly, the reflectivity is reduced to about half. Further, light is absorbed by the black pigment contained in the light shielding films 48, and accordingly, reflected light is also reduced. Therefore, the regular reflection at the display screen is reduced as a whole, and the unclear display due to mirror imaging is improved.

[0088] When low-melting-point glass was not mixed in the light shielding films 48, the regular refractive index was approximately 8% (4% at the glass outer surface and 4% at the phase boundary). When low-melting-point glass powder was mixed into the light shielding films 48, regular refractive index was reduced to about 6% (4% at the glass outer surface and 2% at the phase boundary).

[0089] As is described above, the light shielding films are formed to increase the contrast for a display screen. For this formation, an oxide agent is mixed in the organic photosensitive resist 71 to prevent a color change from occurring during the annealing process, and the low-melting-point glass is mixed in to prevent regular reflection.

[0090] As a method for preventing the change in the color of the light shielding films, proposed is a method wherein the display electrodes are coated with a thin insulation film, such as SiO_2 film, to keep the light shielding films from contacting the display electrodes.

[0091] Fig. 13 is a cross sectional view of a modification of the PDP, showing a front glass substrate 11 and a rear glass substrate 12. In this modification, as light shielding films 48, light shielding films 48A are formed on the outer surface of the front substrate 11 in the areas between the display lines L; light shielding films 48B are formed inside a dielectric layer 17; and light shielding films 48C are formed above a phosphors film 24 on the rear glass substrate 21. Films 48A are not, of course, in accordance with the present invention.

[0092] Regardless of the locations at which the light shielding films 48 are formed, light from the phosphors film 24 can be prevented from leaking out to the front.

[0093] According to embodiments of the present invention, non-luminous areas between display lines can be shielded so they are not noticeable, and the contrast for a display can be increased.

[0094] According to these embodiments, reflection of

external light at the surface of a phosphors layer can be prevented to varying extents, and a display having high contrast can be provided.

[0095] According to these embodiments, reflection of external light can be prevented not only at the area between the display line but also at the surface of a metal electrode, and a display having high contrast can be achieved.

[0096] According to these embodiments, expansion of light shielding films may be prevented in the process for forming a dielectric layer, and reduction of luminance can be prevented.

[0097] According to the above embodiments, since light shielding films can be formed without increasing the number of mask alignment processes for patterning, a high yield can be maintained and the contrast for a display can be increased.

[0098] According to the above embodiments, after display electrodes are formed, light shielding films and a dielectric layer can be formed and annealed together, and a comparatively stable process can be performed.

Claims

1. A surface discharge plasma display panel, having a front substrate (11) and a rear substrate (21) with a discharge space (30) therebetween, and a plurality of pairs of display electrodes (X, Y) extending along respective display lines (L), wherein a reverse slit (S2) where no surface discharge occurs is defined between each adjacent pair of display electrodes (X, Y) and a discharge slit (S1) for surface discharge is defined between display electrodes (X, Y) of each single pair thereof, and further wherein a plurality of phosphors (28) extending in bands are provided, and a plurality of address electrodes (A) are provided on the rear substrate (21), with the phosphors (28) and address electrodes (A) extending along directions crossing the direction of extent of the plurality of pairs of display electrodes (X, Y), the surface discharge plasma display panel further comprising light shielding means (45 to 49) for shielding light hitting the front substrate (11),

   characterised in that the display electrodes (X, Y) are formed on the front substrate (11), the phosphors (28) are provided on the rear substrate (21), and the light shielding means (45 to 49) is a light shielding film positioned between the front substrate (11) and the phosphors (28), the light shielding film extending in bands which have the same direction of extent as the display electrodes (X, Y) and which are arranged at the reverse slits (S2) for shielding light penetration between the front substrate (11) and the rear substrate (21).

2. The surface discharge plasma display panel of claim 1, wherein said light shielding film (45 to 49) has a darker colour than said phosphors (28).

3. The surface discharge plasma display panel of claim 1 or 2, further comprising:

   a dielectric layer (17) formed on the front substrate (11) to cover the display electrodes (X, Y);

   wherein the light shielding film (45, 46, 48, 49) is formed between the front substrate (11) and the dielectric layer (17).

4. The surface discharge plasma display panel of claim 1 or 2, further comprising:

   a dielectric layer (17) formed on the front substrate (11) to cover the display electrodes (X, Y);

   wherein the light shielding film (47) is provided at an intermediate portion in the thickness direction of the dielectric layer (17) and is separated from the display electrodes (X, Y).

5. The surface discharge plasma display panel of any one of the preceding claims, wherein

   each display electrode (X, Y) includes a transparent layer (41) and conductive layer (42), and

   the light shielding film (45 to 49) is made of a material darkened by the inclusion of at least one of Mn, Fe and Cu, and is located between display electrodes (X, Y) and is separated from the display electrodes (X, Y) by a color change preventing gap therebetween.

6. The surface discharge plasma display panel of any one of claims 1 to 4, wherein

   each display electrode (X, Y) comprises a transparent electrode (41) and a metal electrode (42) having a narrower width than the transparent electrode (41) and overlapping the edge of the transparent electrode (41) close to the reverse slit (S2), and

   the light shielding film is provided on the display electrode to overlap the metal electrodes (42) at both sides of the reverse slit (S2).

7. The surface discharge plasma display panel of any one of claims 1 to 4, wherein said display electrodes (X, Y) are provided to partially overlap the light shielding film (45 to 49).

8. The surface discharge plasma display panel of any one of claims 1 to 4, wherein the light shielding film (45 to 49) is provided to contact the reverse slit side edges of said display electrodes (X, Y).

9. The surface discharge plasma display panel of any one of claims 1 to 4, wherein the light shielding film (45 to 49) is provided spaced apart from said display electrodes (X, Y).

10. The surface discharge plasma display panel of any one of claims 1 to 4, wherein the light shielding film (45 to 49) is provided to partially overlap said display electrodes (X, Y).

11. The surface discharge plasma display panel of any one of the preceding claims, wherein a portion of said light shielding film (45 to 49) is provided at a peripheral area of an effective display area of the surface discharge plasma display panel.

12. The surface discharge plasma display panel of any one of the preceding claims, wherein said front substrate (11) is a glass substrate, and the light shielding film (45 to 49) includes glass material.

13. The surface discharge plasma display panel of any one of the preceding claims, further comprising:

a plurality of barrier ribs (29) provided between adjacent address electrodes (A), and the phosphor bands (28) being formed between adjacent barrier ribs (29) to cover the address electrodes (A),

wherein the barrier ribs (29) include a top portion that is darker than the phosphors (28), and a lattice-shaped dark pattern is provided by a combination of the light shielding film (45 to 49) and the barrier ribs (29) crossing each other, to clarify the boundaries of plural display points (R, B, G etc) which constitute each display line (L).

14. The surface discharge display panel of claim 3, wherein the light shielding film (45, 46, 48, 49) is made of a material darkened by the inclusion of at least one of Mn, Fe and Cu.

15. The surface discharge display panel of claim 14, wherein the light shielding film (45, 46, 48, 49) is kept from contacting the display electrodes (X, Y) through an insulating layer which is formed on the display electrodes (X, Y).

Patentansprüche

1. Oberflächenentladungs-Plasmaanzeigefeld, aufweisend ein vorderes Substrat (11) und ein hinteres Substrat (21) mit einem Entladungsraum (30) dazwischen und mehrere Paare Anzeigeelektroden (X, Y), die entlang jeweiligen Anzeigezeilen (L) verlaufen, worin ein Sperrschlitz (S2), wo keine Oberflächenentladung auftritt, zwischen jedem benachbarten Paar Anzeigeelektroden (X, Y) definiert ist und ein Entladungsschlitz (S1) für eine Oberflächenentladung zwischen Anzeigeelektroden (X, Y) von jedem einzelnen Paar davon definiert ist, und worin ferner mehrere, in Bändern verlaufende Leuchtstoffe (28) vorgesehen sind und mehrere Adreßelektroden (A) auf dem hinteren Substrat (21) vorgesehen sind, wobei die Leuchtstoffe (28) und Adreßelektroden (A) entlang Richtungen verlaufen, die die Verlaufsrichtung der mehreren Paare Anzeigeelektroden (X, Y) kreuzen, welches Oberflächenentladungs-Plasmaanzeigefeld ferner ein lichtabschirmendes Mittel (45 bis 49) zum Abschirmen von auf das obere Substrat (11) treffendem Licht aufweist,

dadurch gekennzeichnet, daß die Anzeigeelektroden (X, Y) auf dem vorderen Substrat (11) gebildet sind, die Leuchtstoffe (28) auf dem hinteren Substrat (21) gebildet sind und das lichtabschirmende Mittel (45 bis 49) ein zwischen dem vorderen Substrat (11) und den Leuchtstoffen (28) angeordneter lichtabschirmender Film ist, welcher lichtabschirmende Film in Bändern verläuft, welche die gleiche Verlaufsrichtung wie die Anzeigeelektroden (X, Y) haben und welche an den Sperrschlitzen (S2) angeordnet sind, um eine Lichtdurchdringung zwischen dem vorderen Substrat (11) und dem hinteren Substrat (21) abzuschirmen.

2. Oberflächenentladungs-Plasmaanzeigefeld nach Anspruch 1, worin der lichtabschirmende Film (45 bis 49) eine dunklere Farbe als die Leuchtstoffe (28) hat.

3. Oberflächenentladungs-Plasmaanzeigefeld nach Anspruch 1 oder 2, ferner aufweisend:

eine dielektrische Schicht (17), die auf dem vorderen Substrat (11) gebildet ist, um die Anzeigeelektroden (X, Y) zu bedecken;

worin der lichtabschirmende Film (45, 46, 48, 49) zwischen dem vorderen Substrat (11) und der dielektrischen Schicht (17) gebildet ist.

4. Oberflächenentladungs-Plasmaanzeigefeld nach Anspruch 1 oder 2, ferner aufweisend:

eine dielektrische Schicht (17), die auf dem vorderen Substrat (11) gebildet ist, um die Anzeigeelektroden (X, Y) zu bedecken;

worin der lichtabschirmende Film (47) an einem Zwischenabschnitt in der Dickenrichtung der dielektrischen Schicht (17) vorgesehen und von den Anzeigeelektroden (X, Y) getrennt ist.

5. Oberflächenentladungs-Plasmaanzeigefeld nach einem der vorhergehenden Ansprüche, worin

jede Anzeigeelektrode (X, Y) eine transparente Schicht (41) und eine leitfähige Schicht (42) enthält; und

der lichtabschirmende Film (45 bis 49) aus einem Material hergestellt ist, das durch den Einschluß zumindest eines von Mn, Fe und Cu verdunkelt ist, und zwischen Anzeigeelektroden (X, Y) liegt und von den Anzeigeelektroden (X, Y) durch eine eine Farbänderung verhindernde Lücke dazwischen getrennt ist.

6. Oberflächenentladungs-Plasmaanzeigefeld nach einem der Ansprüche 1 bis 4, worin

jede Anzeigeelektrode (X, Y) eine transparente Elektrode (41) und eine Metallelektrode (42) aufweist, die eine schmalere Breite als die transparente Elektrode (41) hat und den Rand der transparenten Elektrode (41) nahe dem Sperrschlitz (S2) überdeckt, und

der lichtabschirmende Film auf der Anzeigeelektrode vorgesehen ist, um die Metallelektroden (42) an beiden Seiten des Sperrschlitzes (S2) zu überdecken.

7. Oberflächenentladungs-Plasmaanzeigefeld nach einem der Ansprüche 1 bis 4, worin die Anzeigeelektroden (X, Y) vorgesehen sind, um den lichtabschirmenden Film (45 bis 49) teilweise zu überdekken.

8. Oberflächenentladungs-Plasmaanzeigefeld nach einem der Ansprüche 1 bis 4, worin der lichtabschirmende Film (45 bis 49) vorgesehen ist, so daß er die Seitenränder des Sperrschlitzes der Anzeigeelektroden (X, Y) berührt.

9. Oberflächenentladungs-Plasmaanzeigefeld nach einem der Ansprüche 1 bis 4, worin der lichtabschirmende Film (45 bis 49) von den Anzeigeelektroden (X, Y) beabstandet vorgesehen ist.

10. Oberflächenentladungs-Plasmaanzeigefeld nach einem der Ansprüche 1 bis 4, worin der lichtabschirmende Film (45 bis 49) vorgesehen ist, so daß er die Anzeigeelektroden (X, Y) teilweise überdeckt.

11. Oberflächenentladungs-Plasmaanzeigefeld nach einem der Ansprüche, worin ein Abschnitt des lichtabschirmenden Films (45 bis 49) an einem Umfangsbereich eines effektiven Anzeigebereichs des Oberflächenentladungs-Plasmaanzeigefeldes vorgesehen ist.

12. Oberflächenentladungs-Plasmaanzeigefeld nach einem der vorhergehenden Ansprüche, worin das vordere Substrat (11) ein Glassubstrat ist und der lichtabschirmende Film (45 bis 49) Glasmaterial enthält.

13. Oberflächenentladungs-Plasmaanzeigefeld nach einem der vorhergehenden Ansprüche, ferner aufweisend:

mehrere, zwischen benachbarten Adreßelektroden (A) vorgesehene Barrierenrippen (29), und welche Leuchtstoffbänder (28) zwischen benachbarten Barrierenrippen (29) ausgebildet sind, so daß sie die Adreßelektroden (A) bedecken,

worin die Barrierenrippen (29) einen oberen Abschnitt enthalten, der dunkler als die Leuchtstoffe (28) ist, und durch Kombination des lichtabschirmenden Films (45 bis 49) und der Barrierenrippen (29), die einander kreuzen, ein gitterförmiges dunkles Muster gebildet wird, um die Grenzen mehrerer Anzeigepunkte (R, B, G etc.) zu verdeutlichen, welche jede Anzeigezeile (L) bilden.

14. Oberflächenentladungs-Plasmaanzeigefeld nach Anspruch 3, worin der lichtabschirmende Film (45, 46, 48, 49) aus einem Material hergestellt ist, das durch den Einschluß zumindest eines von Mn, Fe und Cu verdunkelt ist.

15. Oberflächenentladungs-Plasmaanzeigefeld nach Anspruch 14, worin durch eine isolierende Schicht, welche auf den Anzeigeelektroden (X, Y) geschaffen ist, verhindert wird, daß der lichtabschirmende Film (45, 46, 48, 49) die Anzeigeelektroden (X, Y) berührt.

Revendications

1. Panneau d'affichage par plasma à décharge en surface, qui possède un substrat avant (11) et un substrat arrière (21) ayant entre eux un espace de décharge (30), une pluralité de paires d'électrodes d'affichage (X, Y) s'étendant suivant des lignes d'affichage respectives (L),
où une contre-fente (S2) dans laquelle aucune décharge en surface ne se produit est définie entre chaque paire adjacente d'électrodes d'affichage (X, Y) et une fente de décharge (S1), destinée à produire une décharge en surface, est définie entre les électrodes d'affichage (X, Y) de chaque paire, considérée isolément, de celles-ci, et où, en outre, une pluralité de luminophores (28) s'étendant suivant des bandes est prévue et une pluralité d'électrodes d'adressage (A) est prévue sur le substrat arrière (21), les luminophores (28) et les électrodes d'adressage (A) s'étendant suivant des directions qui coupent la direction d'extension de la pluralité

de paires d'électrodes d'affichage (X, Y), le panneau d'affichage par plasma à décharge en surface comprenant en outre un moyen faisant écran à la lumière (45 à 49) qui sert à faire écran à la lumière venaison frapper le substrat avant (11),

caractérisé en ce que les électrodes d'affichage (X, Y) sont formées sur le substrat avant (11), les luminophores (28) sont prévus sur le substrat arrière (21), et le moyen (45 à 49) faisant écran à la lumière est une pellicule faisant écran à la lumière qui est placée entre le substrat avant (11) et les luminophores (28), la pellicule qui fait écran à fa lumière s'étendant suivant des bandes qui ont la même direction d'extension que les électrodes d'affichage (X, Y) et qui sont disposées au niveau des contre-fentes (52) afin de faire écran à la pénétration de la lumière entre le substrat avant (11) et le substrat arrière (21).

2. Panneau d'affichage par plasma à décharge en surface selon la revendication 1, où ladite pellicule faisant écran à la lumière (45 à 49) possède une couleur plus sombre que lesdits luminophores (28).

3. Panneau d'affichage par plasma à décharge en surface selon la revendication 1 ou 2, comprenant en outre :

une couche diélectrique (17) formée sur le substrat avant (11) afin de couvrir les électrodes d'affchage (X, Y);

où la pellicule faisant écran à la lumière (45, 46, 48, 49) est formée entre le substrat avant (11) et la couche diélectrique (17).

4. Panneau d'affichage par plasma à décharge en surface selon la revendication 1 ou 2, comprenant en outre :

une couche diélectrique (17) formée sur le substrat avant (11) afin de couvrir les électrodes d'affichage (X, Y);

où la pellicule faisant écran à la lumière (47) est prévue en une position intermédiaire dans la direction d'épaisseur de la couche diélectrique et est séparée des électrodes d'affichage (X, Y).

5. Panneau d'affichage par plasma à décharge en surface selon l'une quelconque des revendications précédentes, où :

chaque électrode d'affichage (X, Y) comporte une couche transparente (41) et une couche conductrice (42), et
la pellicule faisant écran à la lumière (45 à 49) est faite d'une matière obscurcie par inclusion d'au moins l'une des substances Mn, Fe et Cu et est placée entre les électrodes d'affichage (X, Y) et séparée des électrodes d'affichage (X, Y) par un intervalle d'empêchement de changement de couleur se trouvant entre elle.

6. Panneau d'affichage par plasma à décharge en surface selon l'une quelconque des revendications 1 à 4, où chaque électrode d'affichage (X, Y) comprend une électrode transparente (41) et une électrode métallique (42) ayant une largeur plus étroite que l'électrode transparente (41) et chevauchant le bord de l'électrode transparente (41) à proximité de la contre-fente (S2), et

la pellicule faisant écran à la lumière est disposée sur l'électrode d'affichage de façon à chevaucher les électrodes métalliques (42) des deux côtés de la contre-fente (S2).

7. Panneau d'affichage par plasma à décharge en surface selon l'une quelconque des revendications 1 à 4, où lesdites électrodes d'affichage (X, Y) sont disposées de façon à chevaucher partiellement la pellicule faisant écran à la lumière (45 à 49).

8. Panneau d'affichage par plasma à décharge en surface selon l'une quelconque des revendications 1 à 4, où la pellicule faisant obstacle à la lumière (45 à 49) est disposée de façon à être en contact avec les bords latéraux de la contre-fente desdites électrodes d'affichage (X, Y).

9. Panneau d'affichage par plasma à décharge en surface selon l'une quelconque des revendications 1 à 4, où la pellicule faisant écran à la lumière (45 à 49) est disposée de façon à être écartée desdites électrodes d'affichage (X, Y).

10. Panneau d'affichage par plasma à décharge en surface selon l'une quelconque des revendications 1 à 4, où la pellicule faisant écran à la lumière (45 49) est disposée de façon à chevaucher partiellement lesdites électrodes d'affichage (X, Y).

11. Panneau d'affichage par plasma à décharge en surface selon l'une quélconque des revendications précédentes, où une partie de ladite pellicule faisant écran à la lumière (45 à 49) est disposée en une zone périphérique d'une zone d'affichage effective du panneau d'affichage par plasma à décharge en surface.

12. Panneau d'affichage par plasma à décharge en surface selon l'une quelconque des revendications précédentes, où ledit substrat avant (11) est un substrat de verre, et la pellicule faisant écran à la lumière (45 à 49) comporte un matériau du type verre.

13. Panneau d'affichage par plasma à décharge en surface selon l'une quelconque des revendications précédentes, comprenant en outre

une pluralité de nervures constituant des barrières (29) placées entre électrodes d'adressage adjacentes (A), lesdites bandes de luminophores (28) étant formées entre nervures constituant des barrières (29) adjacentes afin de couvrir les électrodes d'adressage (A),
où les nervures constituant des barrières (29) comportent une partie supérieure qui est plus sombre que les luminophores (28), et une configuration sombre en forme de treillis est produite par une combinaison de la pellicule faisant écran à la lumière (45 et 49) et les nervures constituant des barrières (29) se croisant entre elles, afin de clarifier les frontières de plusieurs points d'affichage (R, B, G, etc.) qui constituent chaque ligne d'affichage (L).

14. Panneau d'affichage par plasma à décharge en surface selon la revendication 3, où la pellicule faisant écran à la lumière (45, 46, 48, 49) est faite d'une matière obscurcie par inclusion d'au moins une des substances Mn, Fe et Cu.

15. Panneau d'affichage par plasma à décharge en surface selon la revendication 14, où la pellicule faisant écran à la lumière (45, 46, 48, 49) est empêchée de venir en contact avec les électrodes d'affichage (X, Y) via une couche isolante qui est formée sur les électrodes d'affichage (X, Y).

FIG. 1

BASIC STRUCTURE OF PDP

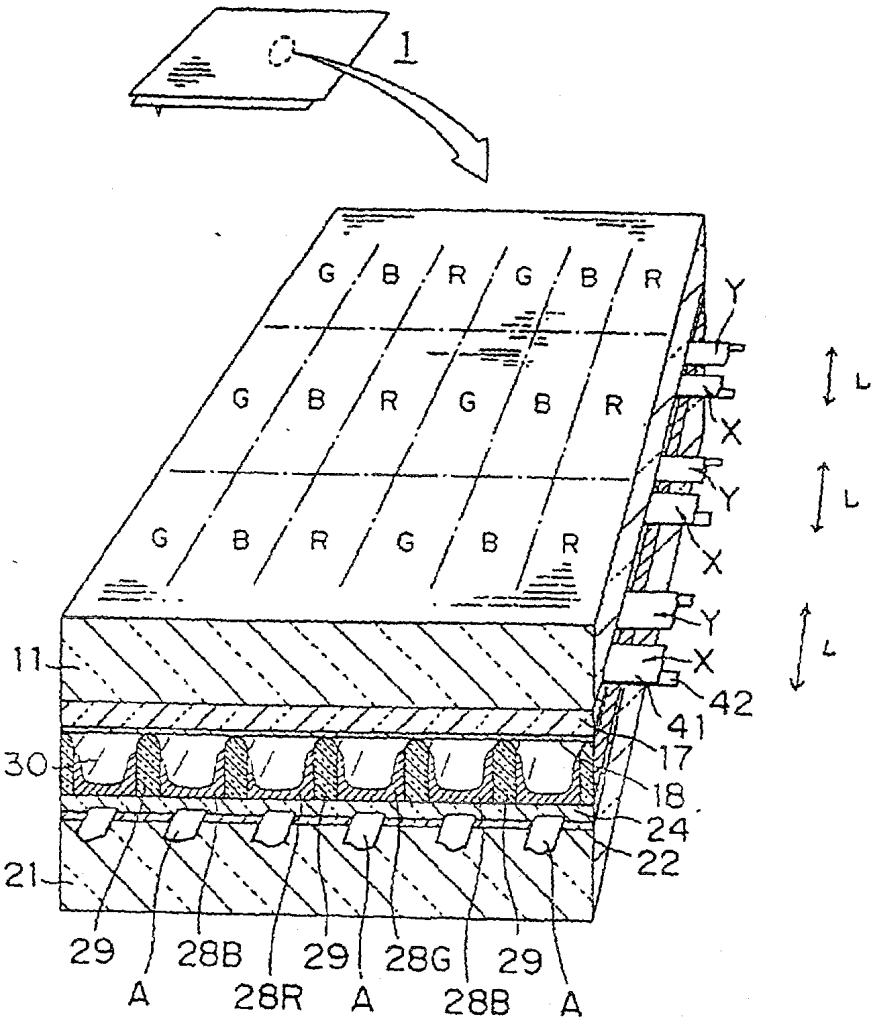


FIG. 2

FIRST EMBODIMENT

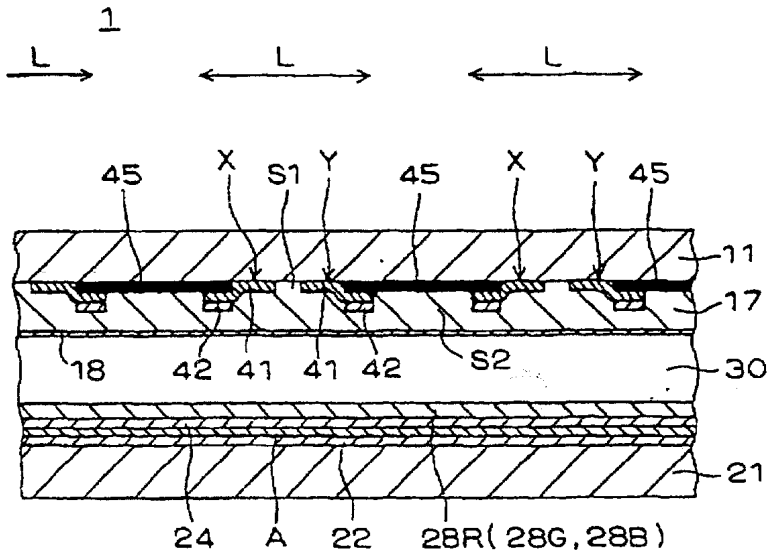


FIG. 3

PLAN VIEW OF LIGHT SHIELDING FILM

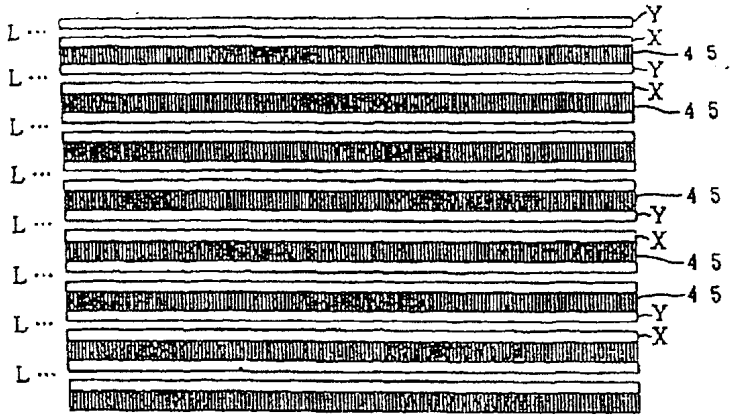


FIG. 4

FABRICATION OF THE FRONT SUBSTRATE

FIG. 4A

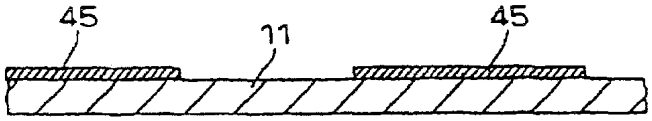


FIG. 4B

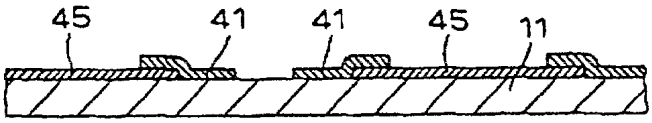


FIG. 4C

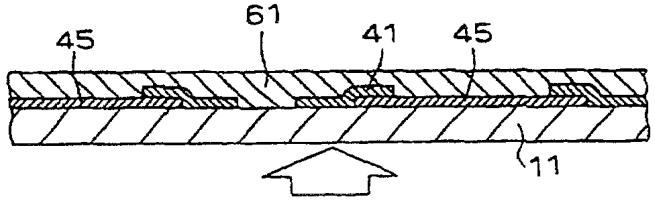


FIG. 4D

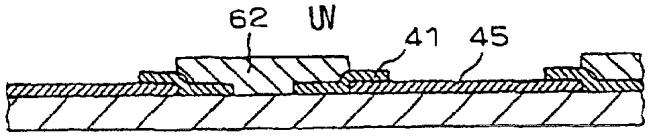


FIG. 4E

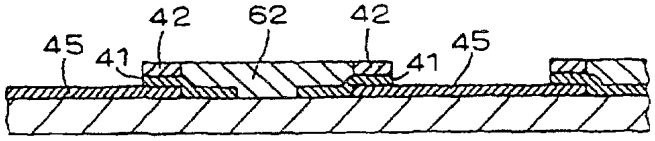


FIG. 4F

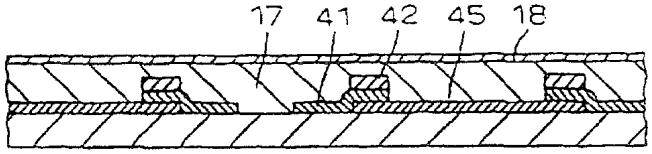


FIG. 5

SECOND EMBODIMENT

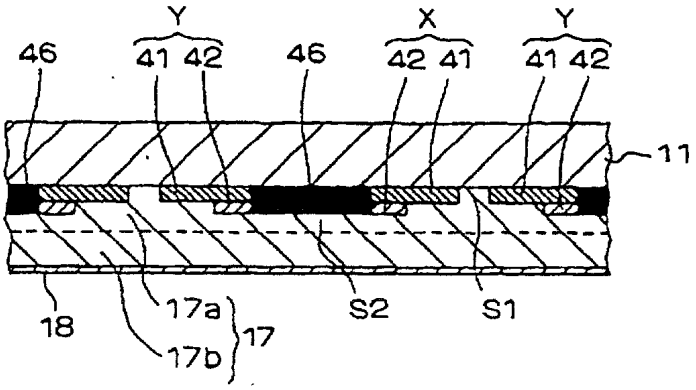


FIG. 6

THIRD EMBODIMENT

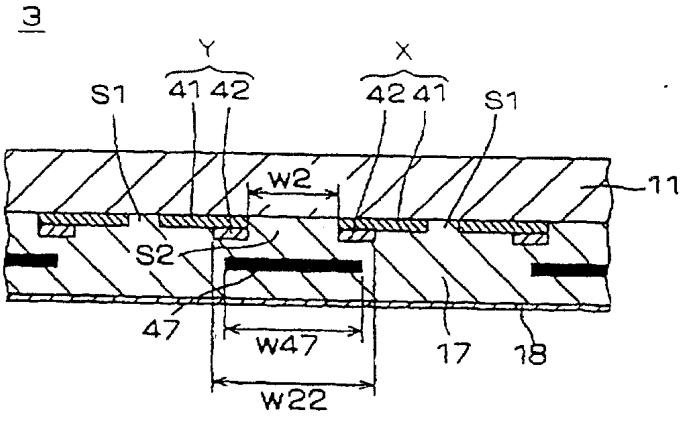


FIG. 7

FOURTH EMBODIMENT

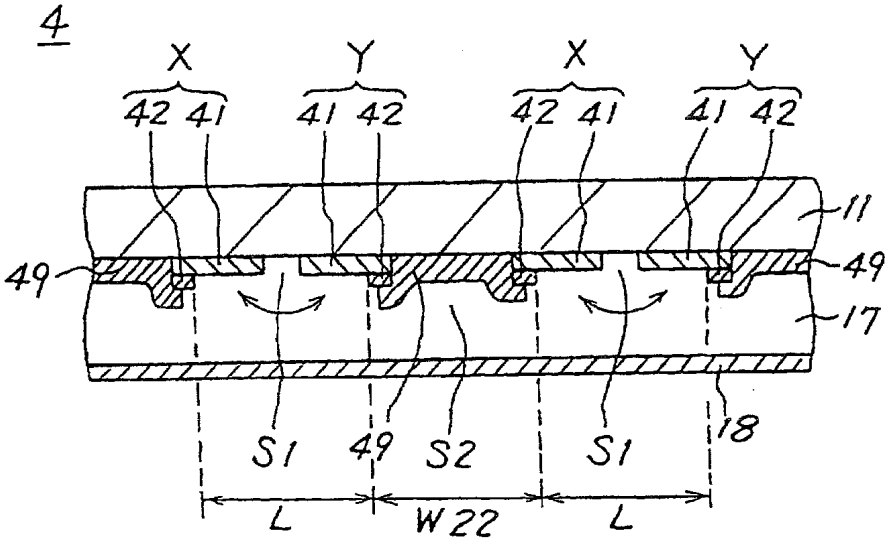


FIG. 8

FIFTH EMBODIMENT

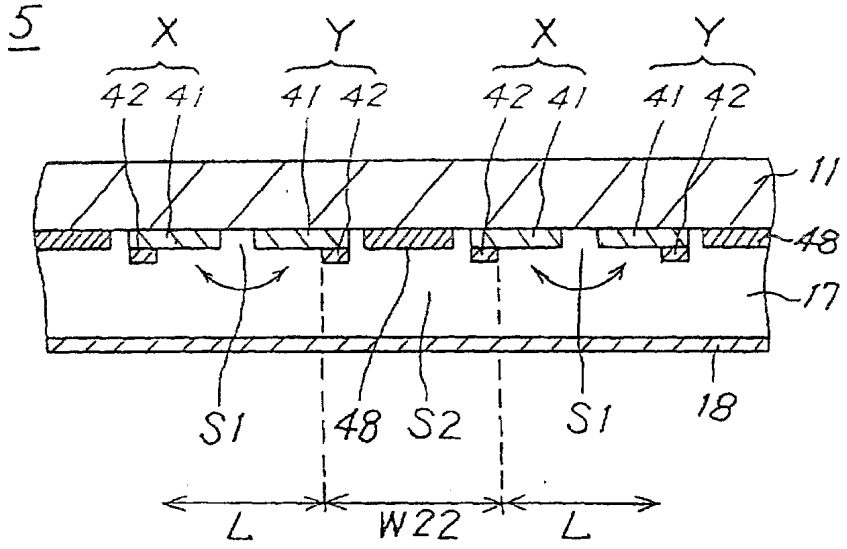


FIG. 9

FABRICATION OF THE FRONT SUBSTRATE

FIG. 9A

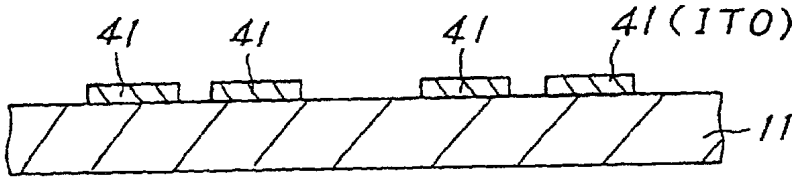


FIG. 9B

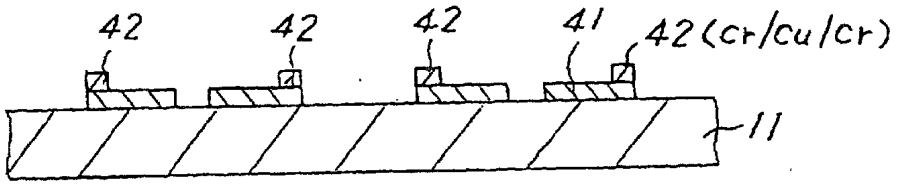


FIG. 9C

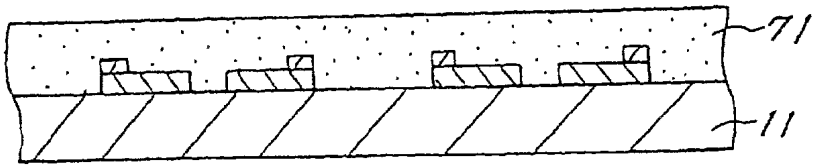


FIG. 9D

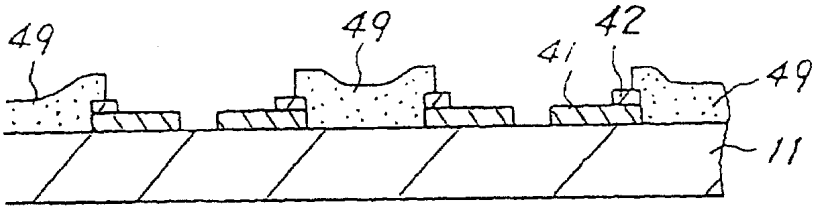


FIG. 9E

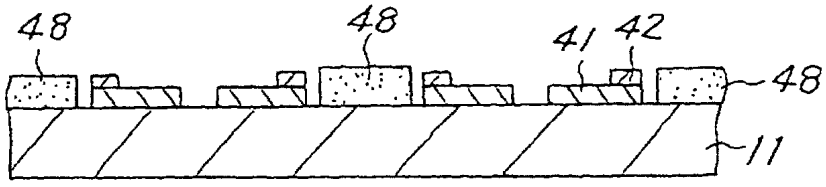


FIG. 10

FABRICATION OF THE FRONT SUBSTRATE

FIG. 10A

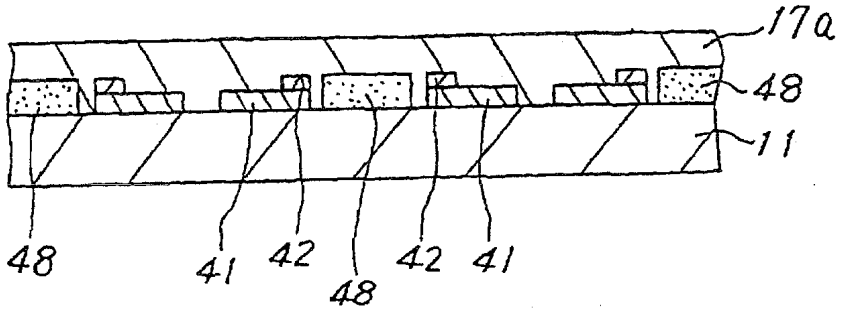


FIG. 10B

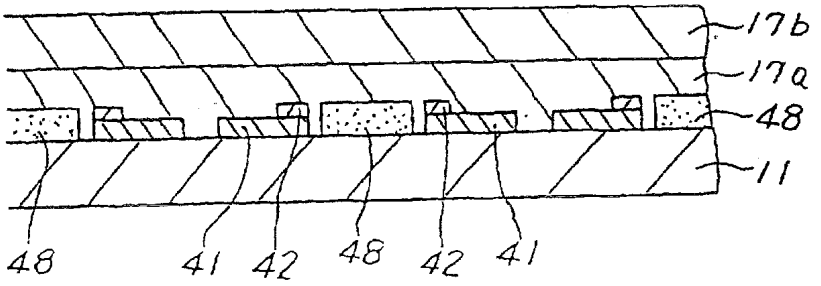


FIG. 10C

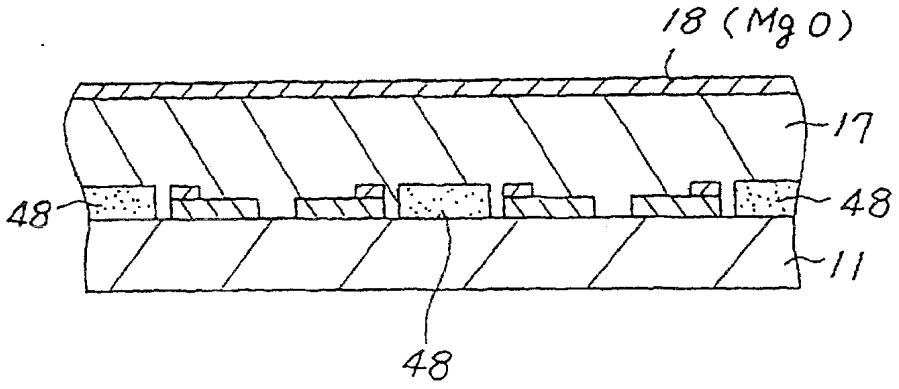
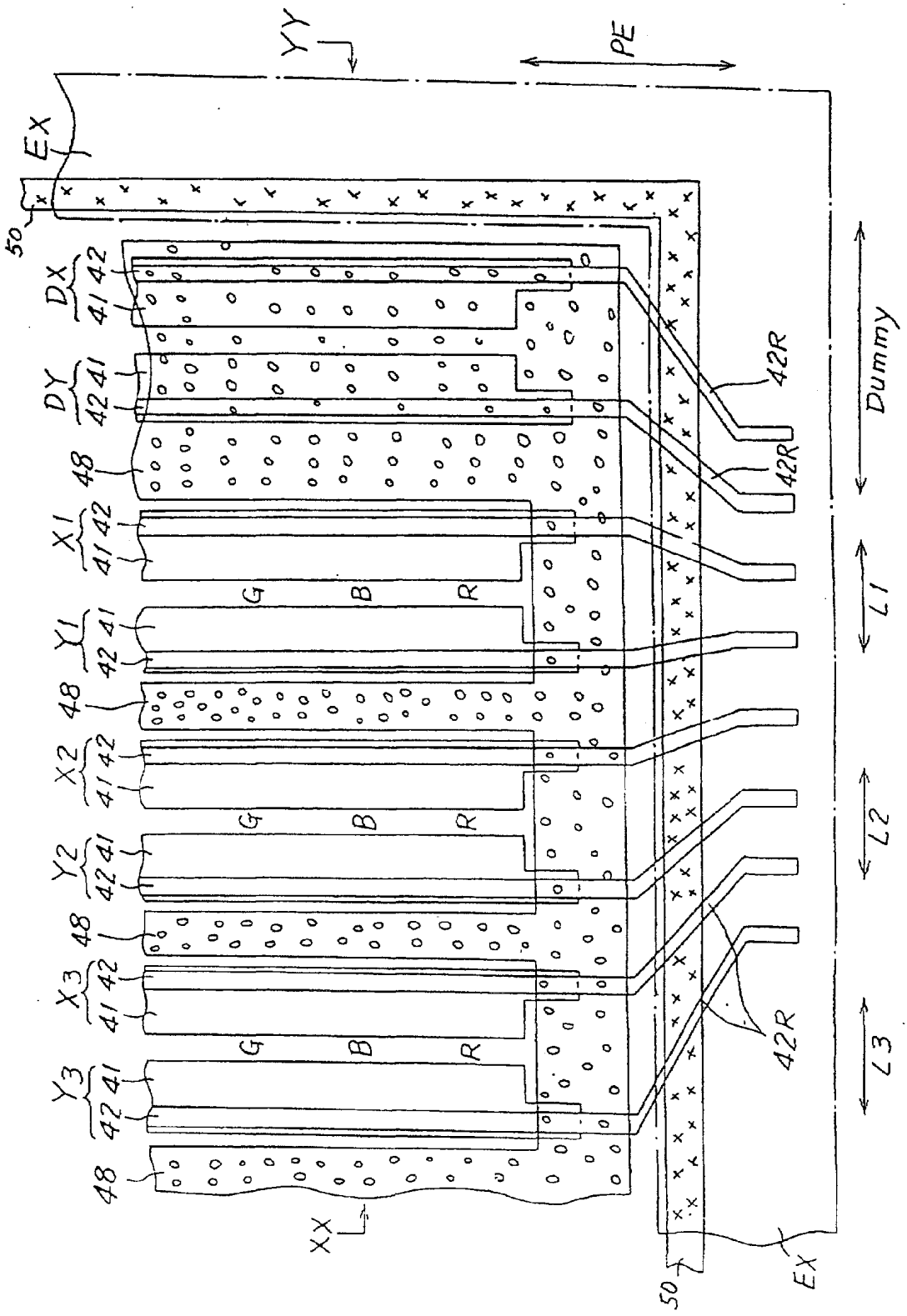


FIG. 11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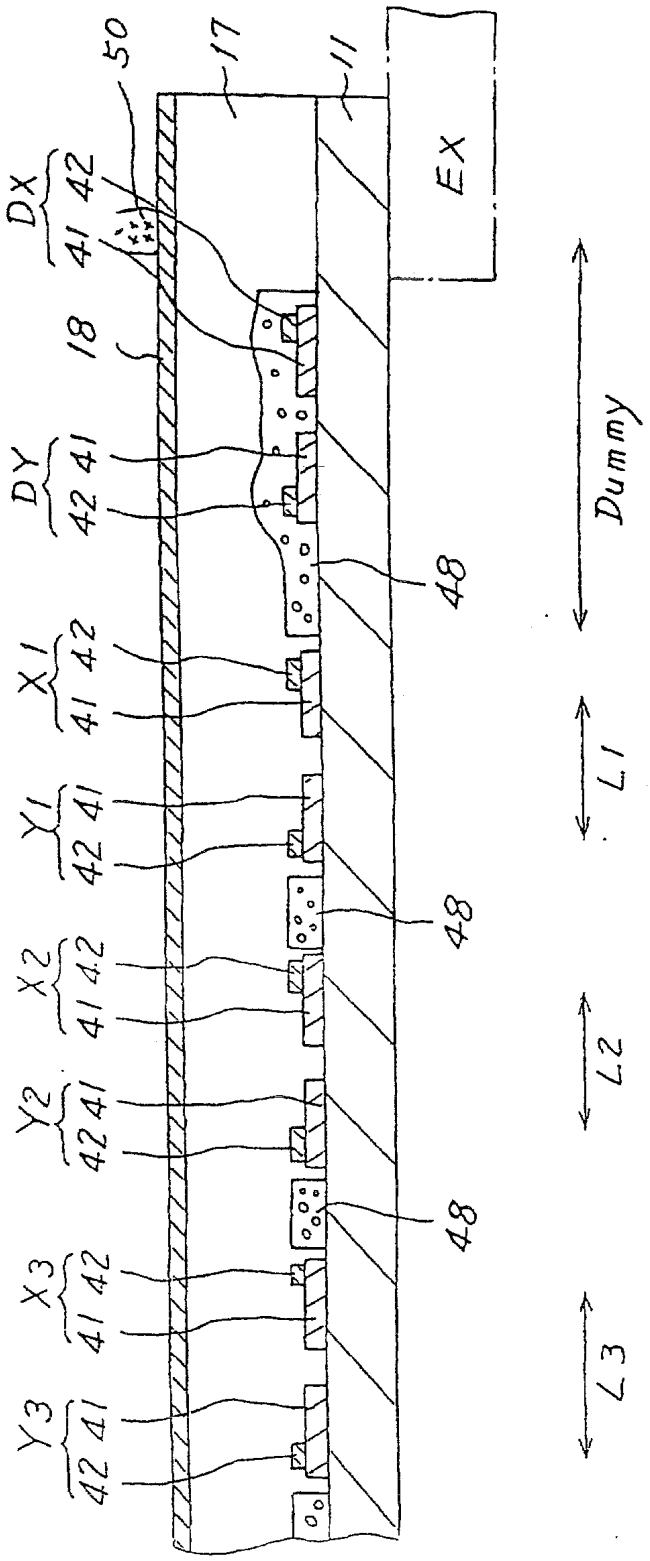
PE
EX
50
DX
41 42
DY
42 41
48
X1
41 42
G
B
R
Y1
42 41
X2
41 42
Y2
42 41
X3
41 42
Y3
42 41
42R
Dummy
L1
L2
L3
XX

FIG. 12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EX
DX
41 42
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DY
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41 42
Y1
42 41
48
X2
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Y2
42 41
48
X3
41 42
Y3
42 41
Dummy
L1
L2
L3

FIG. 13

MODIFICATION

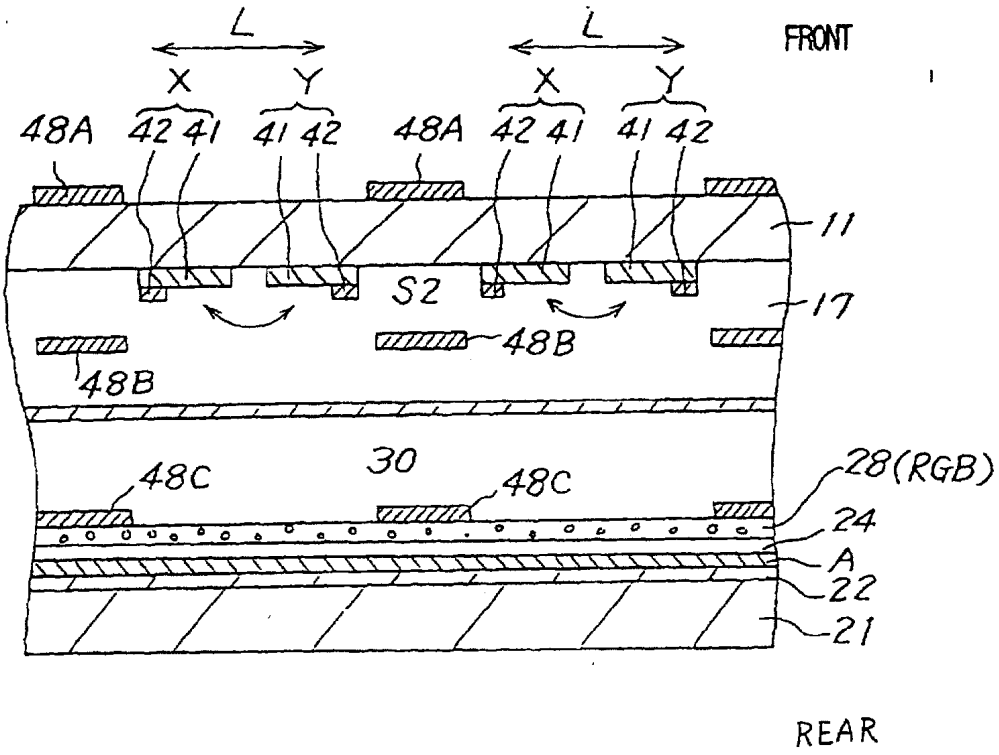

FIG. 14

PRIOR ART PDP